FPGA DESIGN

**PROBLEM STATEMENT:**

To design a **UART** on FPGA using Verilog/VHDL and use it to control a **STOPWATCH** which is also to be implemented on FPGA.

The UART (universal asynchronous receiver and transmitter) module provides asynchronous serial communication with external devices such as modems and other computers The UART can be used to control the process of breaking parallel data from the PC down into serial data that can be transmitted and vice versa for receiving data. The UART allows the devices to communicate without the need to be synchronized.

**Specification:** Main task is to design UART in Verilog/VHDL. After implementing it on FPGA Kit you should be able to communicate your Computer with FPGA Kit. Communication will be done with the help of HyperTerminal program in Computer.

You have to also implement stopwatch on FPGA Kit. Stopwatch will be displayed on LCD.It will have three functionality: Start, Run and Pause. Use PC’S HyperTerminal to send commands to and retrieve time from stopwatch.

**Extra Task:** Modify the stopwatch with an extra feature:

Add an additional signal, **up,** to control the direction of counting. The stopwatch counts up when the **up** signal is asserted and counts down otherwise.